UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,276	02/20/2004	Po-Wei Liu	REAP0050USA	2275

27765   7590   10/31/2007
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EXAMINER
ABRAHAM, ESAW T

ART UNIT	PAPER NUMBER
2112	

NOTIFICATION DATE	DELIVERY MODE
10/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
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PTOL-90A (Rev. 04/07)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amdt filed on 08/21/07*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

- Applicants' response was received on August 21 2007.

- Claim objections are withdrawn in light of amendments/remarks.

- Claim rejections under 35 USC 112 regarding claim 8 is withdrawn.

- Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection under 35 U.S.C. 103(a) as being unpatentable over Brauch et al. (U.S. PN: 6,550,023) in view of Brennan, Ciaran J. (USPUBN: 2005/0138496) further in view of Fukuhisa et al. (US 6,718,496).

Status of claims

- Claims 1-18 stand rejected.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claims 1, 11, 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 11 and 18 recite the phrase "possibly defected memory" is indefinite since the language "possibly" suggests or makes optional and does not limit the scope of a claim.

Applicants are suggested to amend or cancel the claim limitation "possibly".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2.   Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Brauch et al. (U.S. PN: 6,550,023) in view of Brennan, Ciaran J. (USPUBN:

2005/0138496) further in view of Fukuhisa et al. (US 6,718,496).

As per claims 1 and 11 and 18:

Brauch et al. substantially teach or disclose a semiconductor memory testing,

and more particularly to a method and apparatus for testing on-chip RAM and

automatically generating a bitmap indicating cell failures (see col. 1, lines 6-9). Brauch

et al. teach a method and apparatus that makes it possible to detect and locate failing

cells in an integrated circuit memory and further data coming out of the on-chip

memory is compared to its expected value while it is still on-chip and in the event of a

comparison mismatch (or failure), the results of the comparison and its corresponding

address in memory area stored in registers that may be scanned by external hardware and recorded in a bitmap or stored in another on-chip location for later retrieval.

Brauch et al. do not explicitly teach testing the memory under a plurality of operating environments,

However, Brennan in an analogous art teaches a BIST or Built-in self-testing run each set first timing stress on a selected memory cells in a plurality of BISTsequences and run each first set timing stress using <u>different test patterns and/or different conditions that may be selected from a plurality of test sequences</u>. Examples of such plurality of different sequences may be a blanket read pattern, a checker board pattern, a high temperature-low voltage pattern, a low temperature-high voltage pattern and different environmental conditions (see page 3, paragraph 0037).

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include a testing a memory under plurality of environmental conditions as taught by Brennan for testing defected memory. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because testing a defected memory under plurality operating environments improves the efficiency of the test process and accurately analyzes test data and stabilizes the production lines.).

Brauch et al. in view of Brennan do not teach do not teach comparing test results of the plurality of operating environments with one another.

However, Fukuhisa et al. in figure 6 teach a process in which three operating environments are set and three operation voltages are set programmably as an

operation environment. For example, there may be a voltage relation: voltage 3

(136)&;voltage 2 (137)&;voltage 1 (138). That is, voltage 3 is lower than voltage 2, and

voltage 2 is lower than voltage 1. First of all, the memory chip is booted up (step 201)

and the voltage 3 is set (setup 202). Next, the test vector is inputted (step 203). Next,

BIST is performed, <u>the results of BIST are compared with the expected value, and the</u>

<u>results are accumulated (step 204).</u> After BIST, whether the result of BIST is good or

not is decided based on the output of BIST (step 205). The memory should pass in

BISR under voltage 3 if it was determined to be "OK" in step 205. On the other hand,

whether it is repairable or not is decided (step 206) if it was determined to be defective,

that is to say, the defective part is detected in step 205. At this point, the number of

defective parts and the number of redundancy circuits are compared. If the number of

defective parts is fewer than the number of the redundancy circuits, then the memory

chip is considered repairable. However, if the number of defective parts is more than

the number of redundancy circuits, then the memory chip is considered unrepairable

(see col. 5, lines 23-46). Therefore, it would have been obvious to a person having an

ordinary skill in the art at the time the invention was made to compare the testing

results of a testing a memory under plurality of environmental conditions as taught by

Fukuhisa et al. This modification would have been obvious because a person having

ordinary skill in the art would have been motivated to do so because comparing the test

result of operational environment with one another would have improve the efficiency

of the test process.

As per claims 2 and 3:

Brauch et al. teach an integrated circuit (IC) 2 that contains that includes a memory (4), built-in self-test (BIST) (6) and communication port (8). Further, the BIST functional block (6) is hardware, firmware, or a combination of both, that controls the execution of on-chip memory tests that are designed to detect and locate defects in memory (4) (see col. 3, lines 12-48).

As per claims 4 and 5:

Brennan teaches a BIST or Built-in self-testing run each set first timing stress on a selected memory cells in a plurality of BIST sequences and run each first set timing stress using <u>different test patterns and/or different conditions that may be selected from a plurality of test sequences</u>. Examples of such plurality of different sequences may be a blanket read pattern, a checker board pattern, a high temperature-low voltage pattern, a low temperature-high voltage pattern and different environmental conditions (see page 3, paragraph 0037). Further, Fukuhisa et al. teach an operation environment change unit 115 of FIG. 2 changes the environment of the semiconductor device during testing. Changing the operation environment includes a change in operation voltage, a change in operation frequency, a change in operation temperature, and a change in the timing of an input signal. The change in timing of an input signal includes all or partly delaying timing or forwarding timing of the input signals to the semiconductor. Moreover, changing input signal timing includes changing the various input timings of a plurality of input signals (see col. 4, lines 17-26).

As per claims 6-10:

Brauch et al. teach BIST functional block (6) is hardware, firmware, or a combination of both, that controls the execution of on-chip memory tests that are designed to detect and locate defects in memory (4). A fault locator (20) residing within IC 2 performs the comparison between the contents that are read (via data output lines DATA_OUT) and the corresponding expected value. A mismatch between the contents of the addressed location and the expected value indicates a memory defect that corrupts the cell(s) that map to the mismatching bit(s) of the addressed word. Communication port (8)is used to send mismatch address and comparison result pairs off-chip for storage as comparison mismatches are detected. Alternatively, the comparison mismatch information is stored in a bitmap storage (18) located on-chip for later retrieval by external hardware. The accumulated mismatch pairs at the end of the test comprise a complete bitmap of the precise location of failed cells in memory (4) that were detected by the particular memory test executed by BIST functional block (6) (see col. 3, lines 23-46).

As per claims 12 and 13:

Brauch et al. teach a block of an integrated circuit (IC) 2 that contains that includes a memory (4), built-in self-test (BIST) (6) and communication port (8). Further, the BIST functional block (6) is hardware, firmware, or a combination of both, that controls the execution of on-chip memory tests that are designed to detect and locate defects in memory (4) (see col. 3, lines 12-48).

As per claims 14-16:

Brennan teaches a BIST or Built-in self-testing run each set first timing stress on a selected memory cells in a plurality of BISTsequences and run each first set timing stress using different test patterns and/or different conditions that may be selected from a plurality of test sequences. Examples of such plurality of different sequences may be a blanket read pattern, a checker board pattern, a high temperature-low voltage pattern, a low temperature-high voltage pattern and different environmental conditions (see page 3, paragraph 0037). Further, Fukuhisa et al. teach an operation environment change unit 115 of FIG. 2 changes the environment of the semiconductor device during testing. Changing the operation environment includes a change in operation voltage, a change in operation frequency, a change in operation temperature, and a change in the timing of an input signal. The change in timing of an input signal includes all or partly delaying timing or forwarding timing of the input signals to the semiconductor. Moreover, changing input signal timing includes changing the various input timings of a plurality of input signals (see col. 4, lines 17-26).

As per claims 17, 19 and 20:

Fukuhisa et al. in figure 6 teach a process in which three operating environments are set and three operation voltages are set programmably as an operation environment. For example, there may be a voltage relation: voltage 3 (136)&;voltage 2 (137)&;voltage 1 (138). That is, voltage 3 is lower than voltage 2, and voltage 2 is lower than voltage 1. First of all, the memory chip is booted up (step 201) and the voltage 3 is set (setup 202). Next, the test vector is inputted (step 203). Next, BIST is performed, <u>the results of BIST are compared with the expected value, and the results</u>

are accumulated (step 204). After BIST, whether the result of BIST is good or not is decided based on the output of BIST (step 205). The memory should pass in BISR under voltage 3 if it was determined to be "OK" in step 205. On the other hand, whether it is repairable or not is decided (step 206) if it was determined to be defective, that is to say, the defective part is detected in step 205. At this point, the number of defective parts and the number of redundancy circuits are compared. If the number of defective parts is fewer than the number of the redundancy circuits, then the memory chip is considered repairable. However, if the number of defective parts is more than the number of redundancy circuits, then the memory chip is considered unrepairable (see col. 5, lines 23-46). Further, Fukuhisa et al. teach an operation environment change unit 115 of FIG. 2 changes the environment of the semiconductor device during testing. Changing the operation environment includes a change in operation voltage, a change in operation frequency, a change in operation temperature, and a change in the timing of an input signal. The change in timing of an input signal includes all or partly delaying timing or forwarding timing of the input signals to the semiconductor. Moreover, changing input signal timing includes changing the various input timings of a plurality of input signals (see col. 4, lines 17-26).

Conclusion

3.   Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.
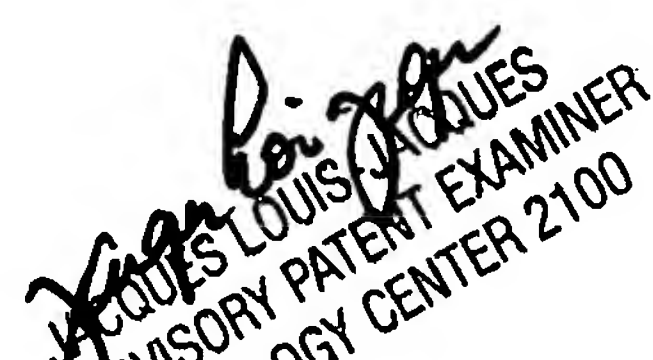
If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham
Esaw Abraham

Art unit: 2112